Introduction

The purpose of this application note is to inform the system designer how to use the HI7190 with a multiplexer. This will enable the designer to perform a high precision 24-bit analog to digital conversion using one sigma delta converter with four fully differential inputs which are individually selectable. Each channel may have a unique gain and filter response as defined by the HI7190 Control Register (CR). Refer to [1] for a complete HI7190 description.

Functional Description

The HI7190 multiplexing circuit is shown in Figure 2. This includes a HI539 4 channel differential multiplexer, two HA5127 single channel ultra-low noise operational amplifiers (op amps) and the HI7190 Sigma-Delta A/D converter.

A fully differential circuit was used to offer the greatest amount of noise immunity and common mode rejection. This type of circuit will only measure the difference between the HI and LO inputs. Noise voltage which is common to both signal lines will cancel out in this balanced differential amplifier. In addition, common mode voltages appearing at the inputs will also be rejected based on the amplifiers Common Mode Rejection Ratio (CMRR). Although differential inputs minimize the effects of noise, proper signal conditioning should be performed (i.e., twisted-pair, isolation, filtering).

The inputs of this circuit begin at the HI539 which is a 4 channel differential multiplexer that has been optimized for low level differential signals. The user selects one of the 4 input channels, labeled CH1 to CH4, based on the multiplexer address A_0 and A_1 (see Table 1 for the address decode). The differential multiplexer outputs labeled OUTA and OUTB are then connected to the non inverting inputs to the HA5127 operational amplifiers. The op amps are used in unity gain to buffer the inputs of the HI7190 and to reduce the loading of the differential input signals being measured. The op amp has been designed for ultra-noise ($3nV/\sqrt{Hz}$) applications and a high CMRR (126dB).

TABLE 1. CHANNEL DECODE

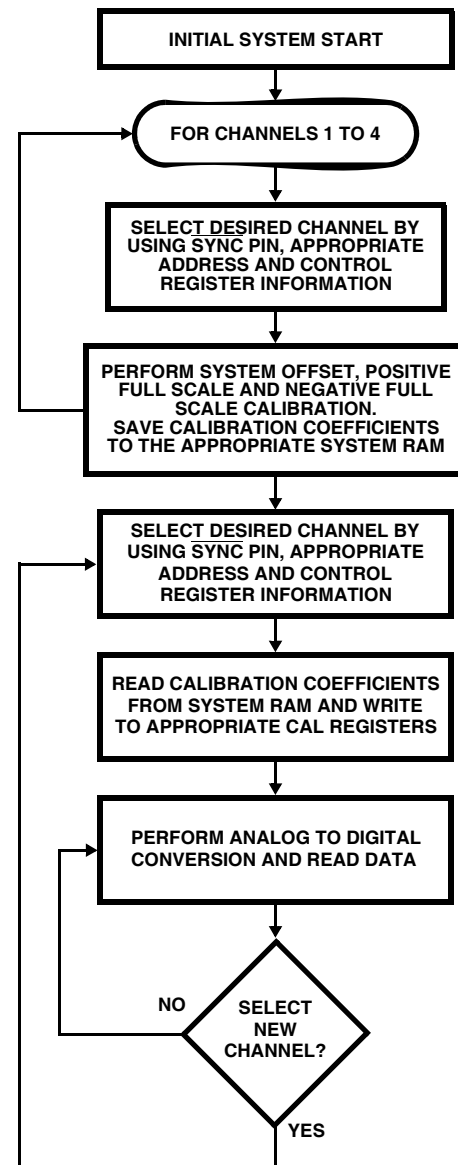| A_1	A_0	SELECTED CHANNEL
0	0	1
0	1	2
1	0	3
1	1	4

FIGURE 1. SYSTEM FLOW CHART

NOTE: Any change in ambient temperature, supply voltage or channel programming (outside of original channel calibration) the user should begin at the "initial system start" block.

Power Supplies

This application circuit is designed to use ±5V for the HI7190 supply and ±10V for the multiplexer and op amps. With these increased op amp supplies, care should be taken to ensure the inputs of the HI7190 do not exceed the HI7190 supplies, or permanent damage may occur.

System Flow and Control

The system flow chart is shown in Figure 1. The details of calibration and channel selection are described in the following sections.

Calibration

The HI7190 has the ability to null any system offset errors and generate the positive and negative gain slope factors for the transfer function of the converter. The system offset and gain errors are nulled by performing a three point calibration which involves recording conversion results for three different input conditions - "zero-scale," "positive full-scale," and "negative full-scale".

Calibration should be performed for EACH of the four channels to null out the individual channel errors with the results stored in the microprocessor memory. When the user switches channels during normal conversions, the calibration coefficients should be read from the microprocessor memory and written back to the HI7190. In addition, the user may have unique gain and filter performance for each channel and restore during the switch. A calibration routine should be initiated whenever there is a change in the ambient operating temperature, supply voltage or any change in the gain, bipolar, or unipolar input range.

Conversion Time

The throughput of the multiplexing application is dependent upon many factors including the programmed notch frequency, input level, settling time of the multiplexer and op amps, serial interface clock and the $\overline{SYNC}$ pin. The $\overline{SYNC}$ pin guarantees a maximum settling time of 3 conversion periods when switching channels of the multiplexer.

The programmed notch frequency defines the number of possible conversions per second. With the default 10MHz crystal the possible notch frequency/conversion rate is 10 to 2000 per second. The input level greatly effects the settling time of the multiplexer, op amps and HI7190. As described in the HI539 and HA5127 datasheets, the multiplexer settles in 0.9μs (0.01%) and op amps settle in 1.5μs (0.1%). The serial interface clock (SCLK) will define the speed of the bit transfer when reading the Control Register and calibration coefficients back to the HI7190 for EACH channel. An active low on the $\overline{SYNC}$ pin is used to reset the modulator and place it in a stand-by mode (not converting) until the pin is returned to high state.

Control/Timing Sequence

To maximize the conversion throughput of this application the user would apply an active low to the $\overline{SYNC}$ pin, change the multiplexer address, write the new channel Control Register and calibration coefficients and return the $\overline{SYNC}$ pin high. Please refer to Figure 3. Below are examples of minimum and maximum conversion rates, assuming a constant channel switching.

Example 1

The notch frequency is programmed for 10Hz, each channel has a unique Control Register (CR), SCLK is in the internal mode of 1.25MHz. The user applies an active low to the $\overline{SYNC}$ pin and changes the multiplexer address. To obtain the new channel information the following bits are transferred from the microprocessor memory. Please refer to the HI7190 datasheet for details of the Serial Interface.

NUMBER OF BITS	REGISTER	COMMENTS
8	IR	Defines pending 3 byte CR write
24	CR	Reprograms the HI7190
8	IR	Defines pending 3 byte offset calibration RAM write
24	OC RAM	Offset calibration coefficients
8	IR	Defines pending 3 byte FS + calibration RAM write
24	FS + RAM	Full scale calibration coefficients
8	IR	Defines pending 3 byte FS - calibration RAM write
24	FS + RAM	Full scale calibration coefficients
128		Total

Given a 1.25MHz SCLK, the bit transfer = 1/SCLK = 800ns. The "reprogramming" would take 800ns x 128 bits = 102μs. The $\overline{SYNC}$ pin can then be returned high since the multiplexer and op amps only needed 0.75μs to switch and 2.4μs to settle but are provided 102μs.

The potential programmed conversion rate of 10Hz equates to 10 conversions per second or one conversion every 100ms; thus implies the 102μs to settle the multiplexer, op amp and reprogramming are negligible. With three conversions needed to stabilize the HI7190, valid results would be available after 300ms. The conversion rate is then 1/300ms or 3.3 conversions per second.

Example 2

The notch frequency is programmed for 2kHz, each channel has a unique Control Register, SCLK is in the external mode with the maximum of 5MHz. The user applies an active low to the $\overline{SYNC}$ pin and changes the multiplexer address. To obtain the new channel information the same 128 bits as described in example 1 are transferred from the microprocessor memory.

Given a 5MHz SCLK the bit transfer = 1/SCLK = 200ns. The "reprogramming" would take 200ns x 128 bits = 26μs. The $\overline{SYNC}$ pin can then be returned high since the multiplexer and op amps only need 0.75μs to switch and 2.4μs to settle but are provided 26μs.

The potential programmed conversion rate of 2kHz equates to 2000 conversions per second or one conversion every 500μs, again implies the 26μs to settle the multiplexer, op amp and reprogramming is negligible.

With three conversions needed to stabilize the HI7190, valid results would be available after 1.5ms. The conversion rate is then 1/1.5ms or 667 conversions per second.

Reference

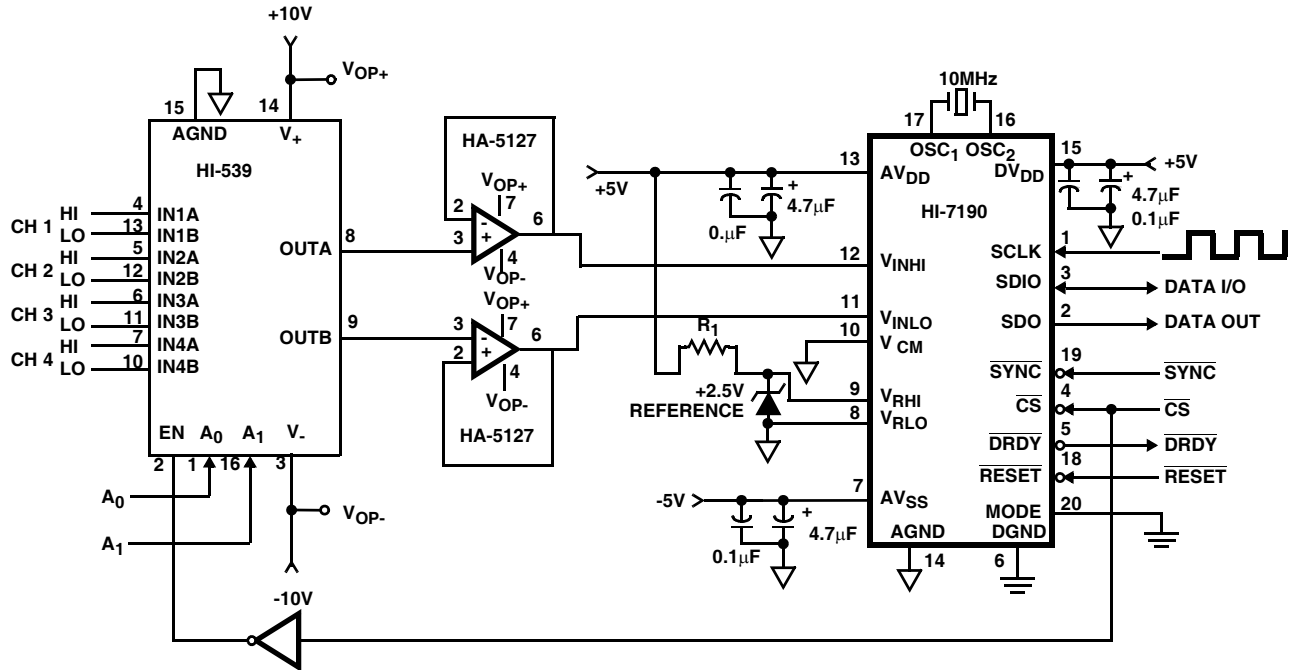[1] HI7190 Data Sheet, FN3612, Intersil Corporation
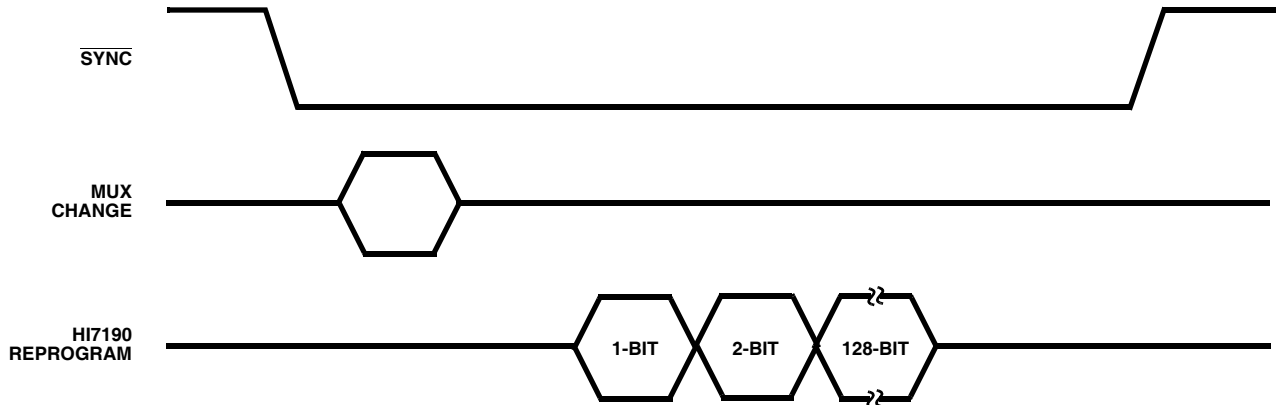

FIGURE 2. MULTIPLEXING CIRCUIT

FIGURE 3. CONTROL SEQUENCE

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